(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 705 051 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
04.04.2001 Bulletin 2001/14

(51) Int Cl.7: **H04Q 11/04**, H04J 3/06, H04L 7/02

(21) Application number: **95202376.0**

(22) Date of filing: **04.09.1995**

(54) Clock recovery for ATM receiver

Taktrückgewinnung für einen ATM-Empfänger

Récupération d'horloge pour un récepteur ATM

(84) Designated Contracting States:
AT BE CH DE DK ES FR GB GR IE IT LI LU NL PT SE

(30) Priority: **21.09.1994 NL 9401525**

(43) Date of publication of application:
03.04.1996 Bulletin 1996/14

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(56) References cited:
EP-A- 0 577 329 **US-A- 4 105 946**

- **OPTICAL ENGINEERING, vol. 28, no. 7, July 1989 BELLINGHAM US, pages 781-788, XP 000033802 H.J.CHAO,C.A.JOHNSTON 'Asynchronous transfer mode packet video transmission system.'**

EP 0 705 051 B1

Printed by Jouve, 75001 PARIS (FR)

Descripti n

A. BACKGROUND OF THE INVENTION

[0001] The invention relates to an ATM receiver, in particular the clock recovery circuit.

[0002] In an ATM transmission system it is possible to transmit, via various virtual channels, source signals at different bit rates, as a result of which the number of ATM cells per unit time, the cell rate, may differ in the one virtual channel from that in another channel. Where the cells of a particular channel arrive at a receiver - allocated temporarily to said channel - said cells must, after having been incorporated in a buffer, be read out therefrom at a clock frequency which is consistent with the cell rate of that channel and with the bit rate (and clock frequency) of the source signal.

[0003] The subject of the present invention is a circuit for deriving, from the cell arrival times, the clock frequency at which said buffer is read out. In the process it is necessary to allow for different nominal cell rates and for variations within those nominal cell rates. So far, the objective of detecting, in a satisfactory manner and entirely automatically, the clock frequency from the arrival times of ATM cells has not been met with a known solution.

B. SUMMARY OF THE INVENTION

[0004] The invention comprises a clock recovery circuit for an ATM receiver, the clock frequency being derived entirely automatically from the cell arrival times. To this end, the circuit according to the invention comprises first means for determining, on the basis of the cell rate of the received cells, the nominal bit rate of the source signal and generating a clock signal having a frequency which is consistent therewith, and second means for correcting, in proportion to the difference between the nominal bit rate determined by the first means and the mean actual bit rate, the frequency of the clock signal generated by the first means. The invention will be expounded hereinafter with reference to a number of figures.

[0005] It is noted that the present application is generally concerned with recovering the receive service clock frequency, as is reference D1. However, the present application addresses a far wider problem than does D1. In that regard, D1 is directed at recovering the receive service clock rate for a single incoming data stream ostensibly transmitted at a ringle rate, i.e., a DS-3 rate, though with some variation, on receive, from that rate. The present application addresses the problem of restoring the receive clock rate across a wide range of predefined clock rates, not just one predefined rate, e. g., a DS-3 rate. The present invention utilizes a totally different approach. The present invention does not -as D1- vary the recovered, i.e., receive, clock rate based on the occupancy of a memory. Rather, the applicant's present invention first sets the frequency of the recovered clock to a predefined value based on a detected nominal bit rate of the incoming data; thus implementing a "coarse" adjustment. Thereafter, this rate is dynamically varied, to effectuate a "fine" adjustment, based on a difference then occurring between a nominal bitrate of incoming data and a mean actual bit rate of that data. Moreover, a system referenced as D2, teaches varying the transmit clock rate based on the number of cells discarded at a receive site, not the receive clock rate.

C. ILLUSTRATIVE EMBODIMENTS

[0006] Figure 1 shows an illustrative embodiment of the invention. Figure 2 depicts a number of signals. Figure 3 shows an illustrative embodiment of one of the units shown in Figure 1.

[0007] The circuit shown in Figure 1 has been designed for automatic recovery of the source clock for source signals having bit rates of 64, 128, 144, 192, 256, 512, 1024 and 2048 kbits/sec. ATM cells are fed to a buffer 1 via an input circuit. By an AND gate 2, a WRITE signal is composed for the cell buffer 1 from a network clock signal of 155.520 MHz (current standard for ATM networks) and a "cell enable" signal by means of which an ATM cell is admitted by the input circuit to buffer 1. Such a "cell enable" signal is produced, for example, by an access monitoring unit such as that described in patent EP - 381 275 B1 in the name of Applicant. The WRITE signal has a "burst" character (see also Figure 2). The rest of the circuit serves to produce a READ clock signal which corresponds to the cell rate of the cells presented to buffer 1 and which does not have a burst character (see also Figure 2). The frequency of that READ signal is equal to the bit rate of the source signal and therefore equal to the frequency of the source clock.

[0008] The circuit includes a coarse adjustment for the clock frequency at which buffer 1 is read out, comprising a division factor adjustment 3 and a variable frequency divider 4. The circuit further includes a fine adjustment, comprising monostable multivibrators 6 and 7, an amplifier 8, a low-pass filter 9, 10 and a VCO (Voltage Controlled Oscillator).

[0009] The division factor adjustment 3 is driven by the "cell enable" signal. After the time between two (or more) successive "cell enable" signals has been measured and the measured time has been categorized in accordance with the closest standard time which corresponds to one of the abovementioned bit rates, a division factor N which has been allocated to that closest standard time is presented to the frequency divider 4. The frequency divider 4 divides the frequency of the clock signal which is presented by the VCO 5 by factor N.

[0010] The variation in cell arrival times (see also Figure 3) must be compensated for by a fine adjustment. To this end, the WRITE signal is also presented to a

monostable multivibrator 7, which assigns a defined width to the WRITE pulses presented. The READ signal is presented to a monostable multivibrator 6 which ensures that the READ pulses are assigned a defined width. The two signals then pass to the + and - input, respectively, of an amplifier 8. At the output a capacitor 10, via a resistor 9, is charged by the READ pulses and discharged by the WRITE pulses. In the case of equilibrium between the number of cells written to the buffer and the number of cells read out, there is equilibrium between charging and discharging of the capacitor 10. If the number of WRITE pulses increases with respect to the number of READ pulses, the voltage $U_{control}$ over capacitor 9 drops, and the frequency of the VCO 5 is readjusted, as a result of which the READ clock frequency increases.

[0011] Figure 3 shows a specific embodiment of the abovementioned unit 3 which calculates the division factor N. This unit comprises a NAND gate 11, a clock generator 12 and a counter 13. Counter 13 receives pulses from clock generator 12 during the period when there is no "cell enable" signal (see also Figure 2). If the cell rate is low, that period is relatively long and the counter attains a relatively high value; at a high cell rate, the counter reaches only a low value. The counter value reached is presented to a number of digital comparators 14 which are each set to a counter value which represents a specific nominal bit rate. The comparator 14 which has a counter value which is closest to the counter value reached by the counter 13 gives an indication to processor 15. Processor 15 calculates, on the basis of the position of that comparator, the value for N and passes this to the variable divider 4. In the case of a low cell rate, the counter 13 reaches a relatively high value, and the value of N likewise becomes relatively high, as a result of which the value of $f \pm \Delta/N$ is relatively low.

D. References

[0012]

D1 Chao, HJ at al, Asynchronous tranfer mode packet video transmission system, Opt. Eng Vol 28 no 7, July 89, pp781-788

D2 US 4 105 946 A in the name of SANSUI ELECTRICH CO. LTD

D3 EP 0 381 275 B1 in the name of KONINKLIJKE PTT NEDERLAND N.V.

Claims

1. Clock recovery circuit for an ATM receiver, for automatically deriving, from the cell rate of received ATM cells, the clock frequency of the source signal, which source signal is transmitted by the ATM cells, characterized by

   first means for determining, (3,4,5) on the basis of the cell rate of the received cells, the nominal bit rate of the source signal and generating a recovered clock signal having a frequency which is consistent therewith, and
   second means (6,7,8,9,10), connected to said first means, for correcting, in proportion to the difference between the nominal bit rate and the mean actual bit rate of the received cells, the frequency of the recovered clock signal generated by the first means.

2. Clock recovery circuit according to Claim 1, characterized in that said first means comprise a division factor unit (3) for determining, on the basis of two or more successive cell arrival times, the nominal bit rate of the source signal transmitted by the ATM cells and generating a division factor (N) as a function of that nominal bit rate, together with a frequency divider (4) for dividing the frequency (f) of a clock signal, which has been output by a clock generator (5), by said division factor.

3. Clock recovery circuit according to Claim 2, characterized by second means which, in proportion to, on the one hand, the number of cell bits received over a period of two or more successive cell arrival time and, on the other hand, the number of clock pulses output by the frequency divider (4) over that same period, output a frequency control signal ($U_{control}$) to said clock generator (5).

4. Clock recovery circuit according to Claim 3, characterized in that clock pulses are presented, in proportion to the cells bits received, to a monostable multivibrator (7) and that the clock pulses output by the frequency divider (4) are presented to an identical monostable multivibrator (6), the output of both said monostable multivibrators being connected to the positive and negative input, respectively, of an amplifier (8) whose output is connected via an integration circuit (9, 10) to the frequency control terminal of a voltage-controlled oscillator (5).

5. Clock recovery circuit according to Claim 1, characterized in that the cell bits of an ATM cell arriving at the receiver are written to a buffer (1) under the control of the network clock signal, while said buffer is read out under the control of the clock signal generated by the first means.

Patentansprüche

1. Taktrückgewinnungschaltkreis für einen ATM-Empfänger, zum vollkommen automatischen Ableiten

der Taktfrequenz des Quellsignals aus der Zellrate von empfangenen ATM-Zellen, wobei das Quellsignal durch die ATM-Zellen übertragen wird, gekennzeichnet durch erste Mittel zur Feststellung (3, 4, 5), auf der Basis der Zellrate der empfangenen Zellen, der nominalen Bit-Rate des Quellsignals und zur Erzeugung eines zurückgewonnenen Taktsignals mit einer Frequenz, die damit übereinstimmend ist, und durch zweite Mittel (6, 7, 8, 9, 10), die mit den ersten Mitteln verbunden sind, zum Korrigieren der Frequenz des zurückgewonnenen Taktsignals, welches vom ersten Mittel erzeugt wird, im Verhältnis zum Unterschied zwischen der nominalen Bit-Rate und der mittleren tatsächlichen Bit-Rate der empfangenen Zellen.

2. Taktrückgewinnungschaltkreis nach Anspruch 1, dadurch gekennzeichnet, dass das erste Mittel eine Teilungsfaktoreinheit (3) zur Feststellung der nominellen Bit-Rate des Quellsignals auf der Basis von zwei oder mehr nacheinander eintreffenden Zellankunftszeiten, welche durch die ATM-Zellen übertragen worden ist und einen Teilungsfaktor (N) erzeugt als Funktion dieser nominellen Bit-Rate, zusammen mit einem Frequenzteiler (4) zum Teilen der Frequenz (f) eines Taktsignals, welches von einem Taktgenerator (5) ausgegeben worden ist, durch diesen besagten Teilungsfaktor.

3. Taktrückgewinnungsschaltkreis nach Anspruch 2, dadurch gekennzeichnet, dass zweite Mittel vorgesehen sind, die in Proportion zu, auf der einen Seite der Anzahl der über eine Periode von zwei oder mehr aufeinanderfolgenden Zellankunftszeiten der Anzahl der Zell-Bits und auf der anderen Seite der Anzahl der Takt-Pulse, die durch den Frequenzteiler (4) über dieselbe Periode ausgegeben werden, ein Frequenzsteuersignal ($U_{control}$) für den besagten Taktgenerator (5) herausgeben.

4. Taktrückgewinnungsschaltkreis nach Anspruch 3, dadurch gekennzeichnet, dass die Takt-Pulse in Proportion zu den empfangenen Zell-Bits einem monostabilen Zellvibrator (7) zugeführt werden und dass die Takt-Pulse, die von dem Frequenzteiler (4) ausgegeben werden, einem identischen monostabilen Multivibrator (6) vorgelegt werden, wobei der Ausgang von beiden besagten monostabilen Multivibratoren mit einem positiven und mit einem negativen Eingang eines Verstärkers (8) verbunden sind, dessen Ausgang über einen Integrationsschaltkreis (9, 10) einem Frequenzsteuerungsabschluss eines spannungsgesteuerten Oszilators (5) verbunden sind.

5. Taktrückgewinnungsschaltkreis nach Anspruch 4, dadurch gekennzeichnet, dass die Zell-Bits einer ATM-Zelle, die an dem Empfänger ankommen, in einen Puffer (1) unter der Steuerung des Netzwerktaktsignals geschrieben werden, während der besagte Puffer unter der Steuerung des Taktsignals ausgelesen wird, das durch die ersten Mittel erzeugt wird.

Revendications

1. Circuit d'extraction de signal d'horloge pour un récepteur ATM, servant à obtenir de façon automatique, à partir du débit de cellules relatif à des cellules ATM reçues, la fréquence d'horloge du signal de source, lequel signal de source est transmis par les cellules ATM, caractérisé par:

   un premier moyen (3, 4, 5) servant à déterminer, sur la base du débit de cellules relatif aux cellules reçues, le débit binaire nominal du signal de source et à produire un signal d'horloge récupéré, ou extrait, possédant une fréquence qui est compatible avec ce débit, et
   un deuxième moyen (6, 7, 8, 9, 10) connecté audit premier moyen et servant à corriger, en proportion de la différence entre le débit binaire nominal et le débit binaire réel moyen des cellules reçues, la fréquence du signal d'horloge récupéré, ou extrait, qui est produit par le premier moyen.

2. Circuit d'extraction de signal d'horloge selon la revendication 1, caractérisé en ce que ledit premier moyen comprend une unité (3) de production de facteur de division servant à déterminer, sur la base de deux ou plus de deux temps d'arrivée de cellules successifs, le débit binaire nominal du signal de source transmis par les cellules ATM et à produire un facteur de division (N) en fonction de ce débit binaire nominal, en même temps qu'un diviseur de fréquence (4) servant à diviser, par ledit facteur de division, la fréquence (f) d'un signal d'horloge, qui a été délivré par un générateur de signal d'horloge (5).

3. Circuit d'extraction de signal d'horloge selon la revendication 2, caractérisé par un deuxième moyen qui, en proportion, d'une part, du nombre de bits de cellules reçus sur un laps de temps de deux ou plus de deux temps d'arrivée de cellules successifs et, d'autre part, du nombre d'impulsions d'horloge délivrées par le diviseur de fréquence (4) sur ce même laps de temps, délivre un signal de commande de fréquence ($U_{commande}$) audit générateur de signal d'horloge (5).

4. Circuit d'extraction de signal d'horloge selon la revendication 3, caractérisé en ce que des impulsions d'horloge sont présentées, en proportion des bits

de cellules reçus. à un multivibrateur monostable (7) et en ce que les impulsions d'horloge délivrées par le diviseur de fréquence (4) sont présentées à un multivibrateur monostable (6) identique, les sorties desdits multivibrateurs monostables étant respectivement connectées à l'entrée positive et à l'entrée négative d'un amplificateur (8) dont la sortie est connectée via un circuit d'intégration (9,10), à la borne de commande de fréquence d'un oscillateur commandé par tension (5).

5. Circuit d'extraction de signal d'horloge selon la revendication 1. caractérisé ce que les bits de cellule d'une cellule ATM arrivant dans le récepteur sont écrits dans un tampon (1) sous commande du signal d'horloge de réseau. tandis que ledit tampon est lu sous commande du signal d'horloge produit par le premier moyen.

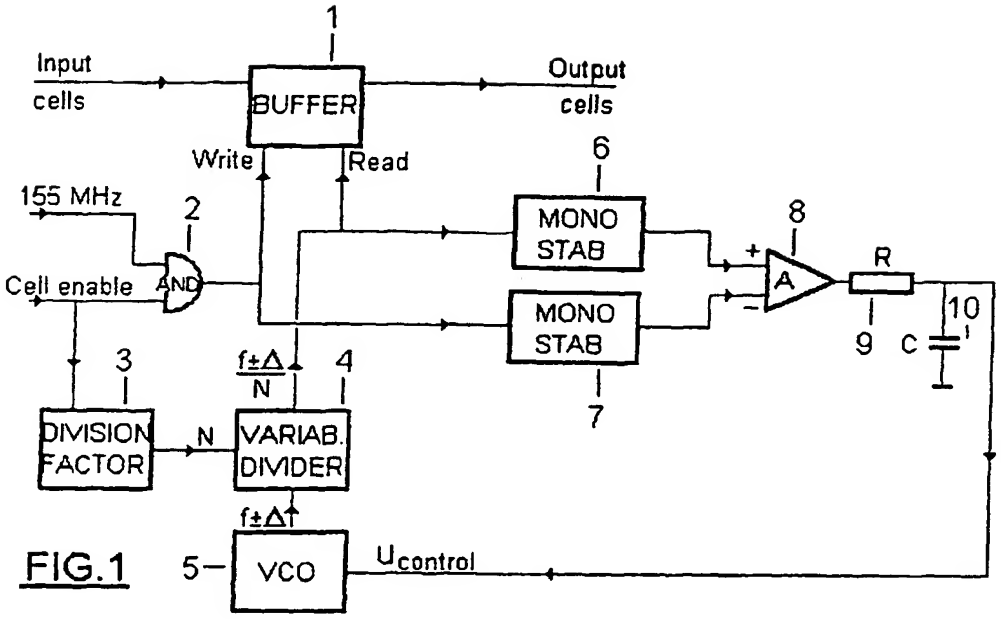
1
Input
cells
BUFFER
Output
cells
Write
Read
6
155 MHz
2
MONO
STAB
8
+
A
R
Cell enable
AND
MONO
STAB
−
9
C
10
3
f±Δ
N
4
7
DIVISION
FACTOR
N
VARIAB.
DIVIDER
f±Δ
5
VCO
Ucontrol

FIG.1

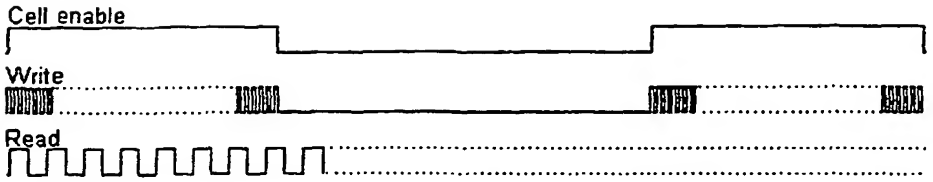
Cell enable
Write
Read

FIG.2

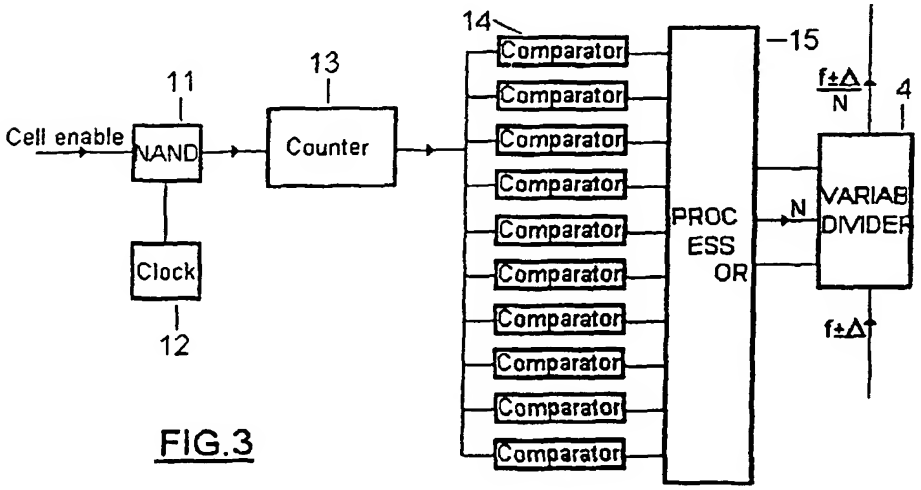
Cell enable
NAND
11
Clock
12
13
Counter
14
Comparator
Comparator
Comparator
Comparator
Comparator
Comparator
Comparator
Comparator
Comparator
Comparator
PROC
ESS
OR
15
N
VARIAB
DIVIDER
f±Δ
N
4
f±Δ

FIG.3